INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, ALLAHABAD,
UTTAR PRADESH, INDIA - 211012

WORKSHOP ON DIGITAL SYSTEMS AND ARCHITECHTURE USING VERILOG

Date: April 5 -7, 2019
Venue: Department of Electronics and Communication Engineering, IIIT - Allahabad

OVERVIEW OF WORKSHOP

The rapid advancement in the digital technology and system integration have made possible to design chips with more than billion transistors. To do so in digital domain, simulation using hardware description language (HDL) is required. Of many existing HDL languages, VERILOG is considered to be one of the preferred language which is also extensively used in Industry/academia for digital embedded systems.

A specialized training program has therefore been designed for digital system architecture using VERILOG targeting in-house and external participants.

IIIT Allahabad UG students and external UG/PG students from other universities, colleges, and institutions will be benefited by this workshop.

TENTATIVE SCHEDULE

Day-1

S.N	Topic	Time	Speaker
1.	Registration and inaugural Session	9:00 am -9:15 am	
2.	Overview of Course, Objective and Latest trends in VLSI Design	9:15 am-10:15 am	IIIT Faculty
	Tea Break~ 10:15 am -10:30 am		
3.	VLSI Design flow, Design styles, Introduction to FPGA (architecture)	10:30 am -11:30	IIIT Fcaulty
4.	Digital Design -1	11:30 -12:30 pm	NXP,Semiconductor,Noida
5.	Digital Design -2	12:30pm-2:30 pm	Qualcomm,Bangalore
	Lunch ~ 2:30pm – 3:00pm		
6.	Lab session	3:00 pm -6:00 pm	

Day-2

S.N	Topic	Time	Speaker
1	Synchronous digital design-1	9:00 am -10:am	IIIT Faculty
2	Synchronous digital design-2	10-11:00 am	IIIT Faculty
3	Tea Break~ 11:00 am -11:15 am		
4	Combinational and Sequential Design	10:30 am -12:30	NXP,Semiconductor,Noida
5	Combinational and Sequential Design	12:30 -2:30 pm	Qualcomm,Bangalore
	Lunch ~ 2:30pm – 3:00pm		
6	Lab session	3:00 pm -6:00 pm	

Day-3

S.N	Topic	Time	Speaker
1	FPGA Architecture & Implementation -1	9:00 am -10:am	IIIT Faculty
2	FPGA Architecture & Implementation -2	10-11:00 am	IIIT Faculty
3	Tea Break~ 11:00 am -11:15 am		
4	Digital System Design	11:15am -6:00pm	Qualcomm,Bangalore

REGISTRATION DETAILS

- Registration fees Rs.2,000/- (including accommodation)
- Fill in the Registration Form available at URL

https://docs.google.com/forms/d/e/1FAIpQLSdabequOGUM6bFsvYFuS6g7LYwK3BWs2Cu0VPzvkJeGBPC4jg/viewform

- The confirmation of registration will be within 5 days of the submission of the form.
- All participants need to send a DD favouring –
  'The Director, IIIT Allahabad' payable at Allahabad, before March 26th, 2019.

OR

The participants can also pay registration fees through Internet transfer of which the details are:
Account Name: Indian Institute of Information Technology
Account Number: 30996838478
IFSC Code: SBIN0010891
Bank & Branch: State Bank of India, Jhalwa, Allahabad

CONTACTS

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